

## ABSTRACT

An ESD protection device having reduced trigger voltage is disclosed. A first  
5 MOS transistor includes a first gate, a first heavily doped region at one side of the first  
gate, and a second heavily doped region at the other side of the first gate. A second  
MOS transistor is laterally disposed in proximity to the first MOS transistor. The  
second MOS transistor includes a second gate, a third heavily doped region at one side  
of the second gate, and a fourth heavily doped region at the other side of the second  
10 gate. The floating gate MOS transistor is located between the first and second MOS  
transistors. A floating gate MOS transistor is serially connected to the first MOS  
transistor via the second heavily doped region and is serially connected to the second  
MOS transistor via the third heavily doped region.

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